EE 434

Lecture 32

Logic Design

Review from last time:

Logic Circuit Block Design

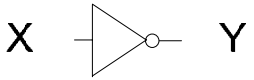
Many different logic design styles

- Static Logic Gates
- Complex Logic Gates
- Pseudo NMOS
- Pass Transistor Logic
- Dynamic Logic Gates
  - Domino Logic
  - Zipper Logic
  - Output Prediction Logic

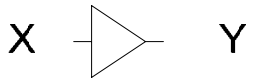
Various logic design styles often combined in the implementation of one logic block

Review from last time:

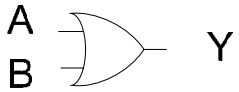
The basic logic gates



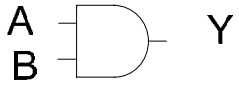
$Y = \overline{X}$



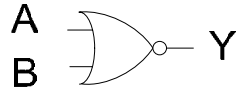
$Y = X$



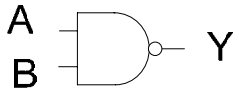
$Y = A + B$



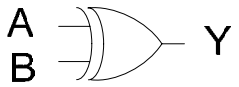
$Y = A \bullet B$



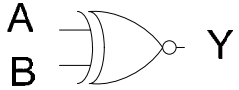
$Y = \overline{A + B}$



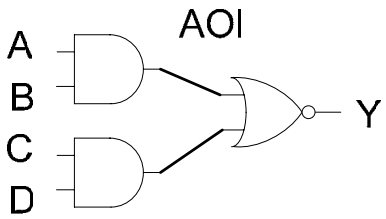
$Y = \overline{A \bullet B}$



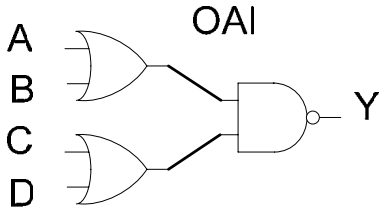
$Y = A \oplus B$



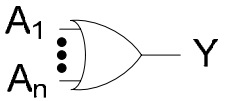
$Y = \overline{A \oplus B}$



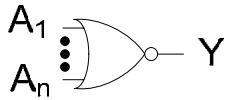
$Y = \overline{A \bullet B + C \bullet D}$



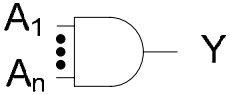
$Y = \overline{(A + B) \bullet (C + D)}$



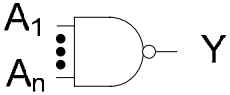
$Y = A_1 + A_2 + \ldots A_n$



$Y = \overline{A_1 + A_2 + \ldots A_n}$



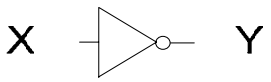
$Y = A_1 \bullet A_2 \bullet \ldots A_n$



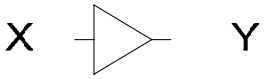
$Y = \overline{A_1 \bullet A_2 \bullet \ldots A_n}$

Review from last time:

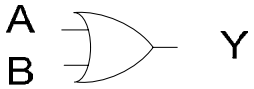
The basic logic gates



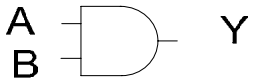
$$Y = \overline{X}$$



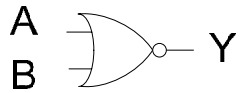
$$Y = X$$



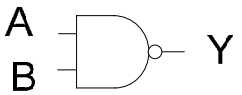
$$Y = A + B$$



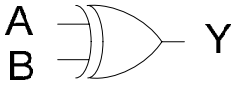
$$Y = A \bullet B$$



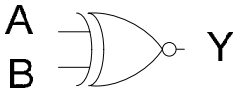
$$Y = \overline{A + B}$$



$$Y = \overline{A \bullet B}$$



$$Y = A \oplus B$$



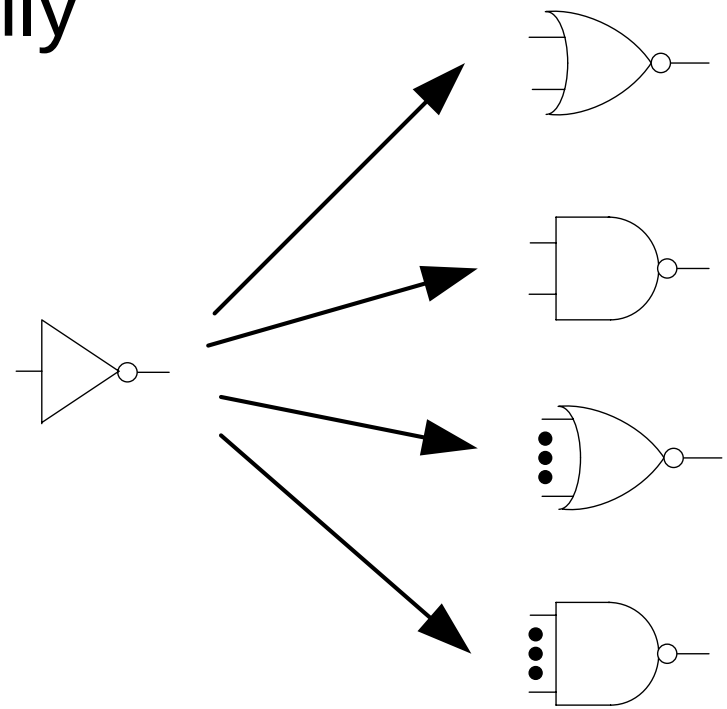
$$Y = \overline{A \oplus B}$$

Question: How many basic one and two input gates exist and how many of these are useful?

Review from last time:

The basic logic gates

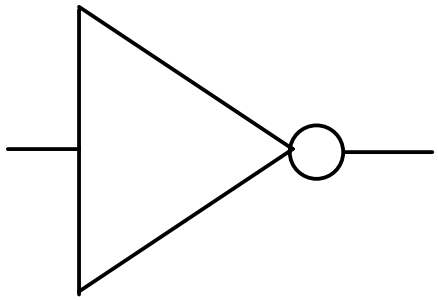
The characteristics of any gate logic family can be expressed rather simply in terms of the characteristics of the basic inverter in that logic family



Review from last time:

The basic logic gates

It suffices to inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

Review from last time:

Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements

Review from last time:

Desirable and/or Required Logic Family Characteristics

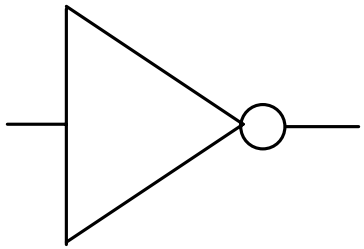
8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

Review from last time:

What are the logic levels for a given inverter of for a given logic family?

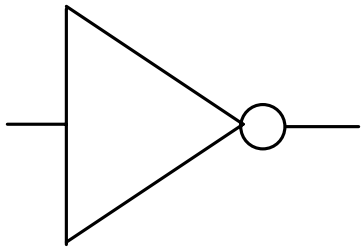


V_H=? V_L=?

Can we legislate them ?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- But what if the circuit does not interpret them the same way they are defined !!

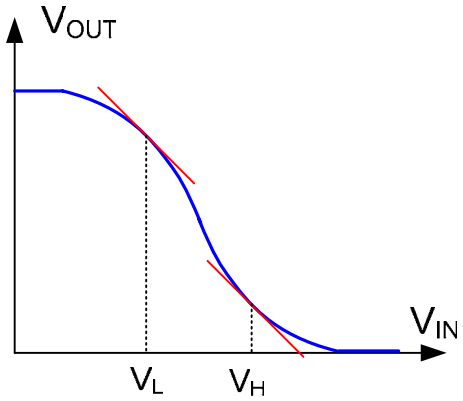
What are the logic levels for a given inverter of for a given logic family?



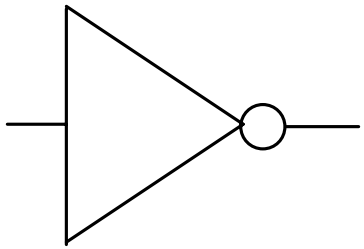
V_H=? V_L=?

Can we legislate them ?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined !!



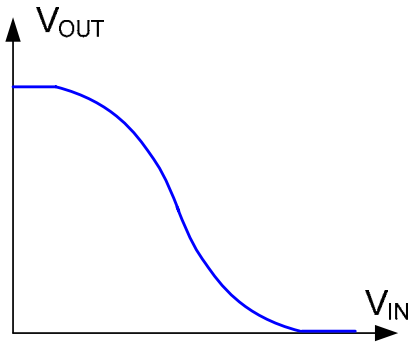
What are the logic levels for a given inverter of for a given logic family?



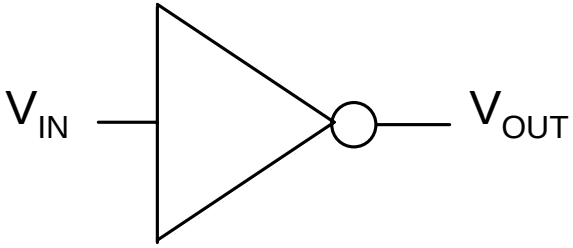
V_H=? V_L=?

Ask the inverter how it will interpret logic levels

- The circuit will interpret them the way they are defined !!
- Analytical expressions may be complicated
- How is this determination made?

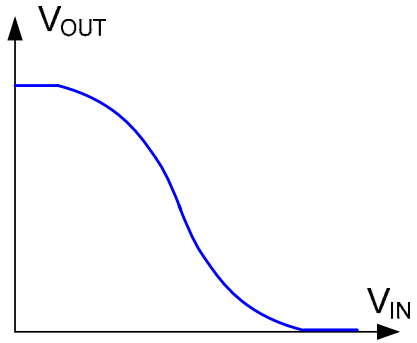


Ask the inverter how it will interpret logic levels



V_H=?

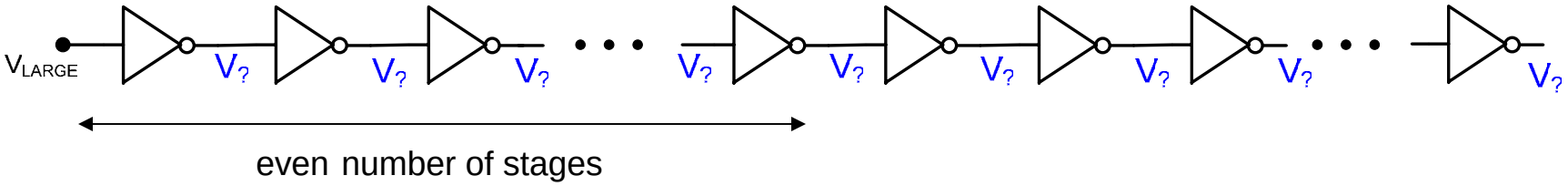
V_L=?



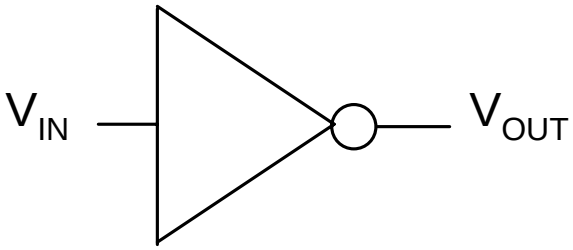
Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated

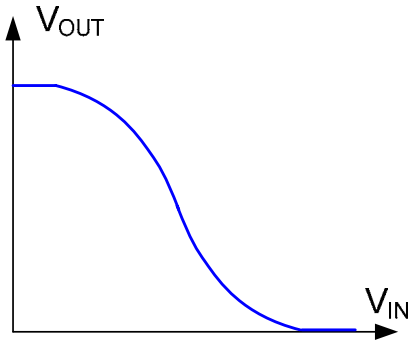


Ask the inverter how it will interpret logic levels



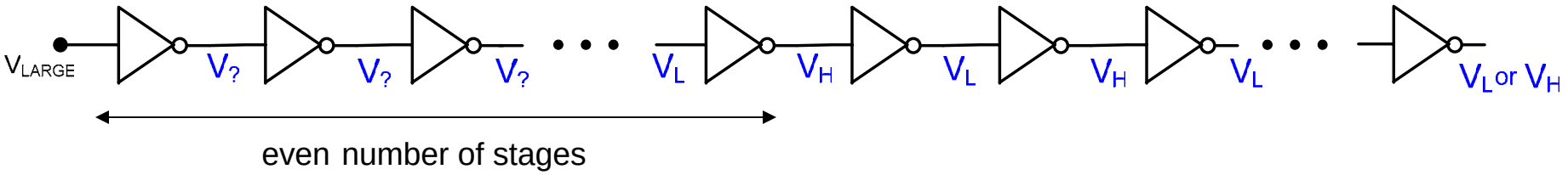
V_H=?

V_L=?



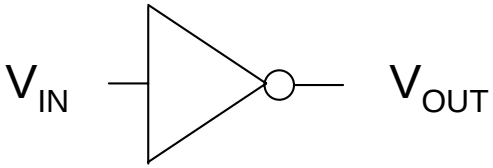
Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)
w.l.o.g. assume an even number of inverters in chain indicated



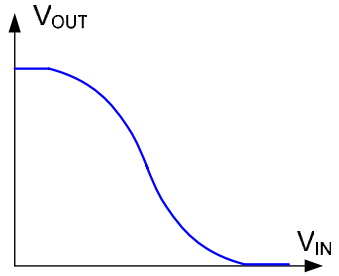
If logic levels are to be maintained, the voltage at the end of this even number of stages must be V_H, that of the next must be V_L, the next V_H, etc. until the end of the cascade is reached

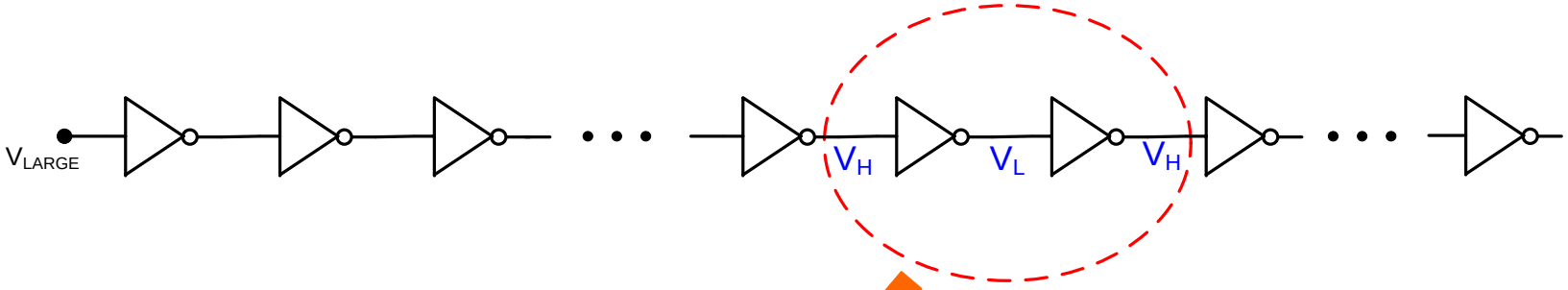
Ask the inverter how it will interpret logic levels

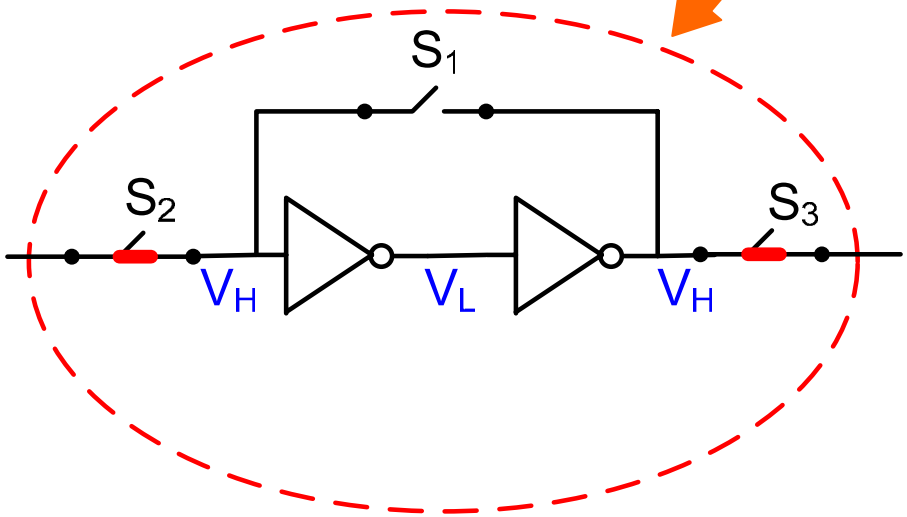


V_H=?

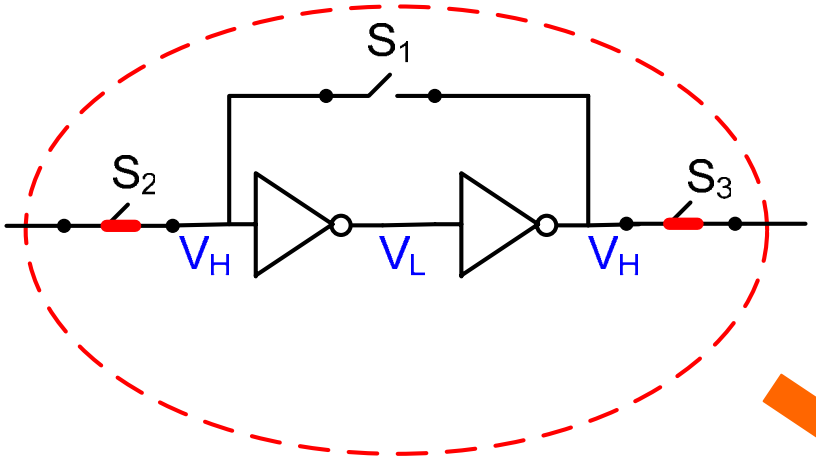
V_L=?

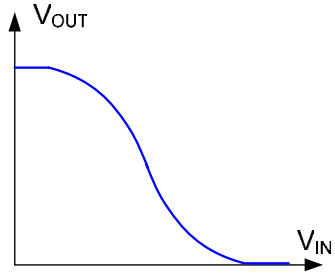






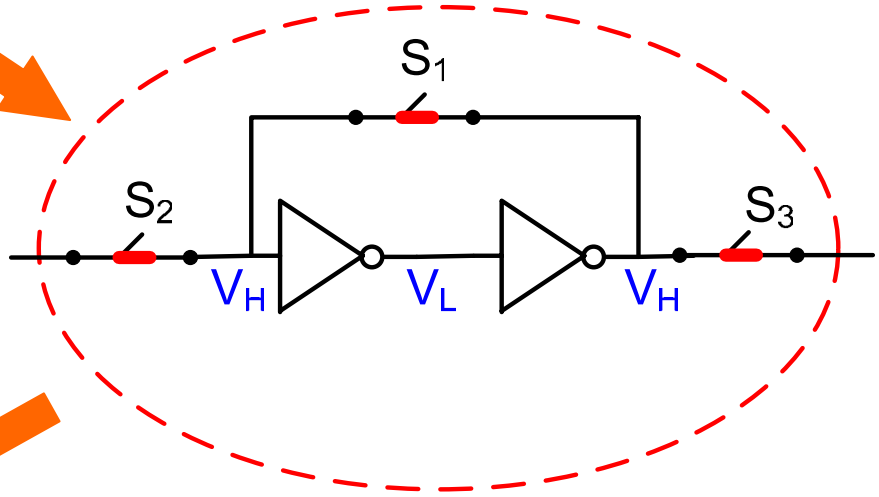
Ask the inverter how it will interpret logic levels

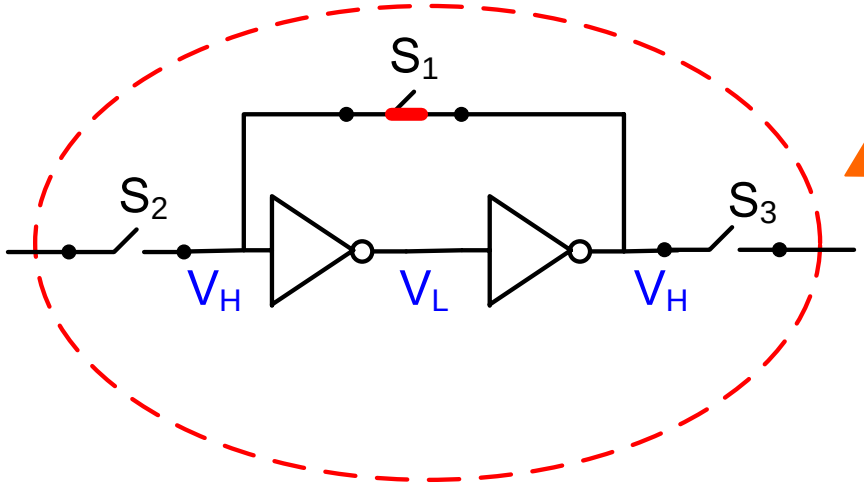




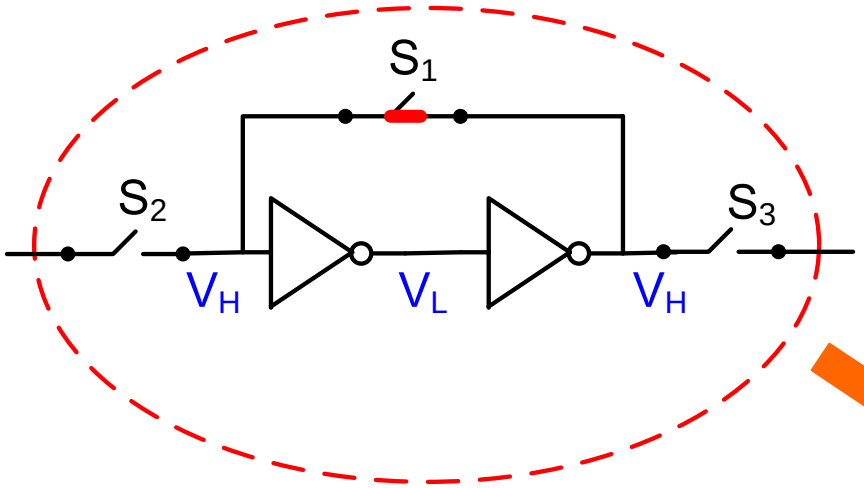
V_H=?

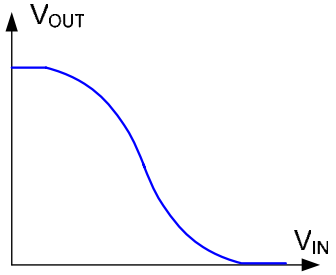
V_L=?





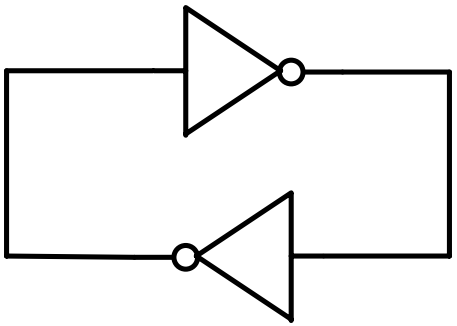
Ask the inverter how it will interpret logic levels





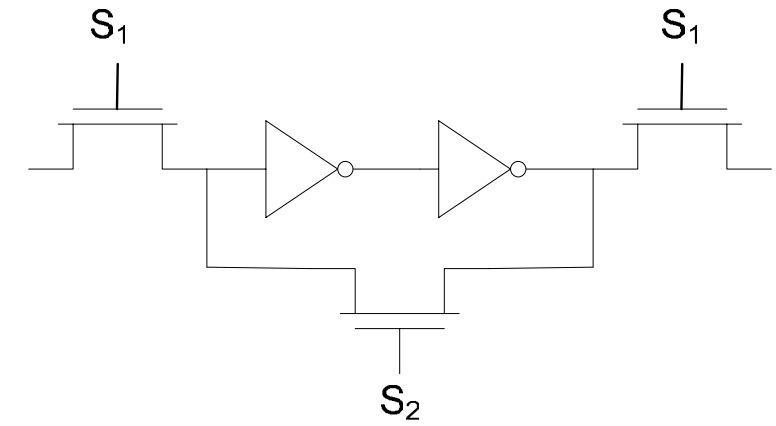
V_H=?

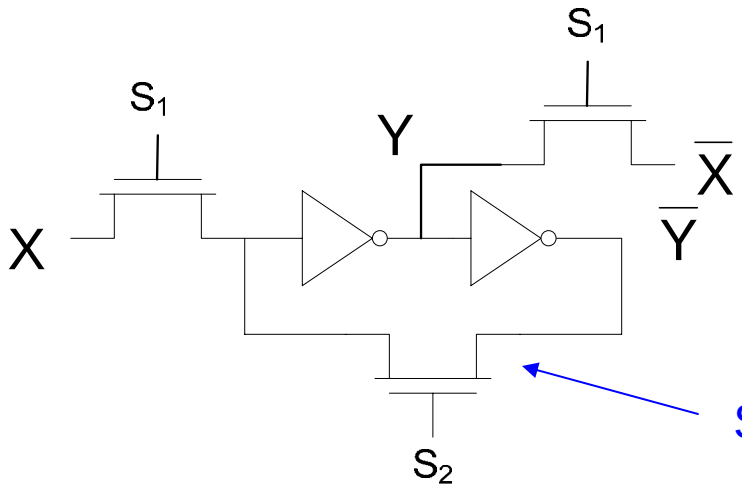
V_L=?



- Two inverter loop
- Very useful circuit !

The two-inverter loop

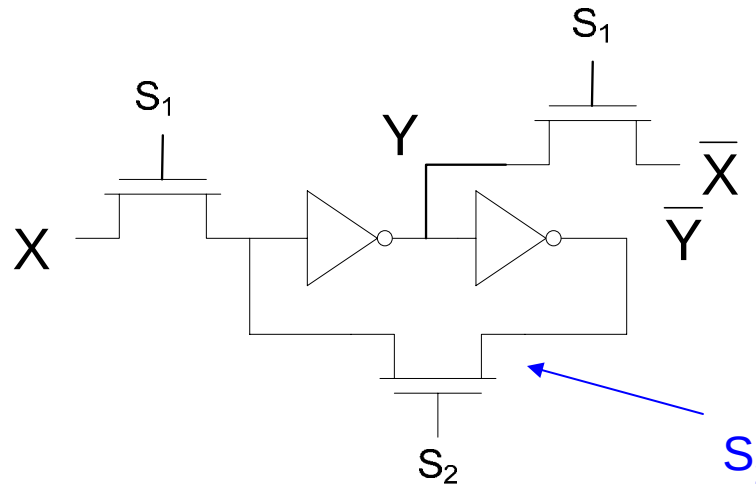




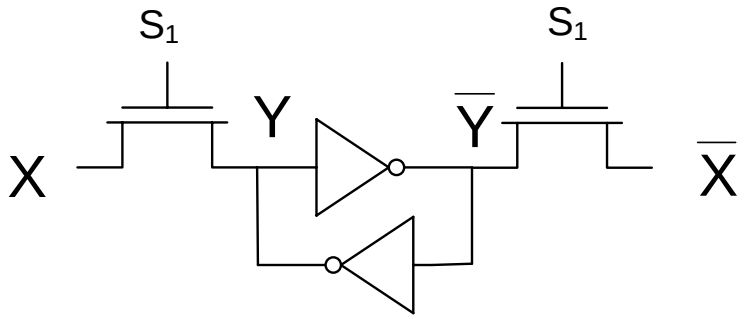
S_2 often eliminated (shorted)

SRAM Cell

The two-inverter loop

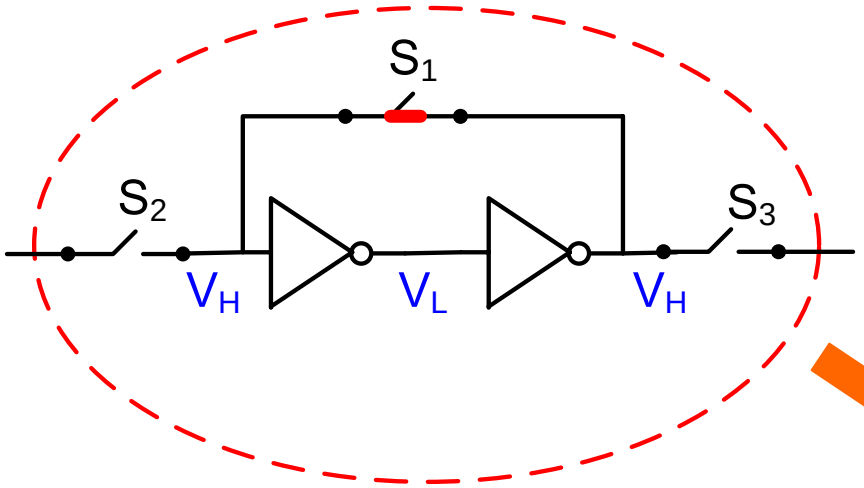


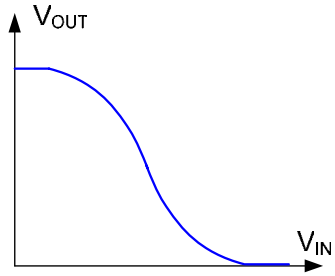
S_2 often eliminated (shorted)



Standard 6-transistor SRAM Cell

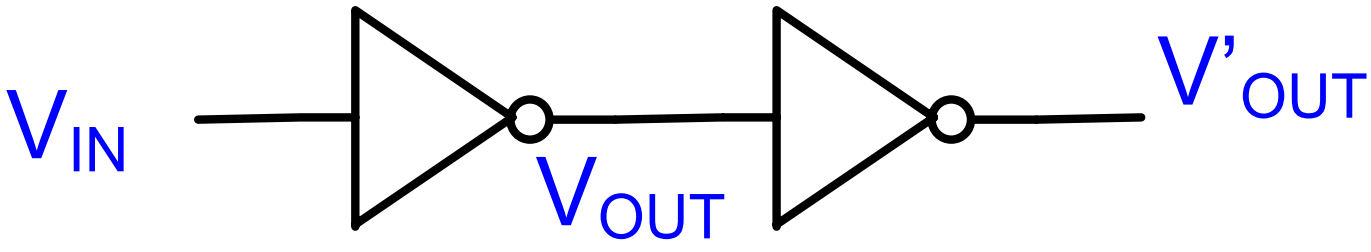
Ask the inverter how it will interpret logic levels





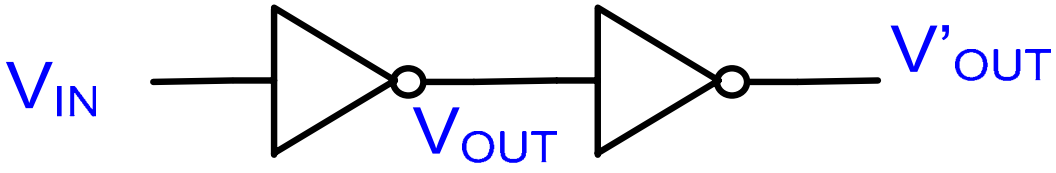
V_H=?

V_L=?

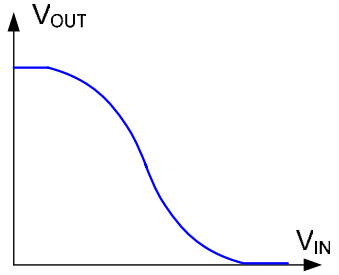


Thus, consider the inverter pair

Ask the inverter how it will interpret logic levels



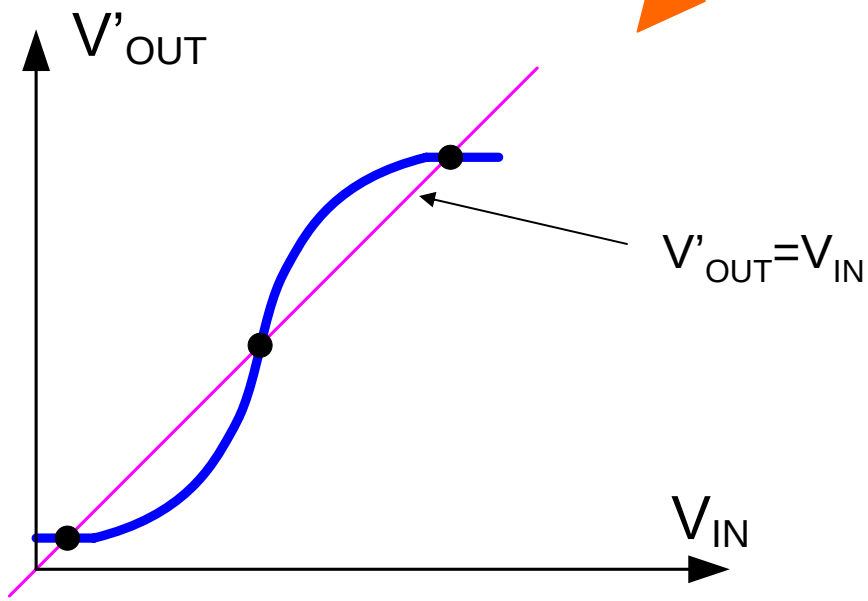
Inverter pair



V_H=?

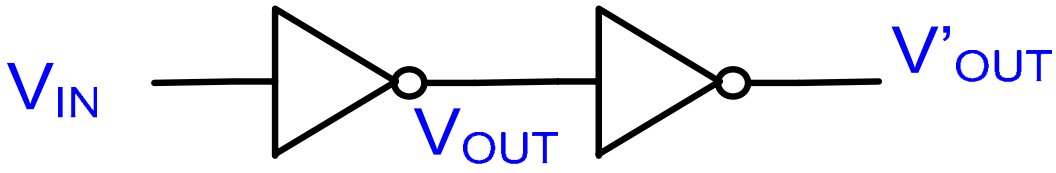
V_L=?

V_H and V_L will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the $V'_{OUT}=V_{IN}$ line

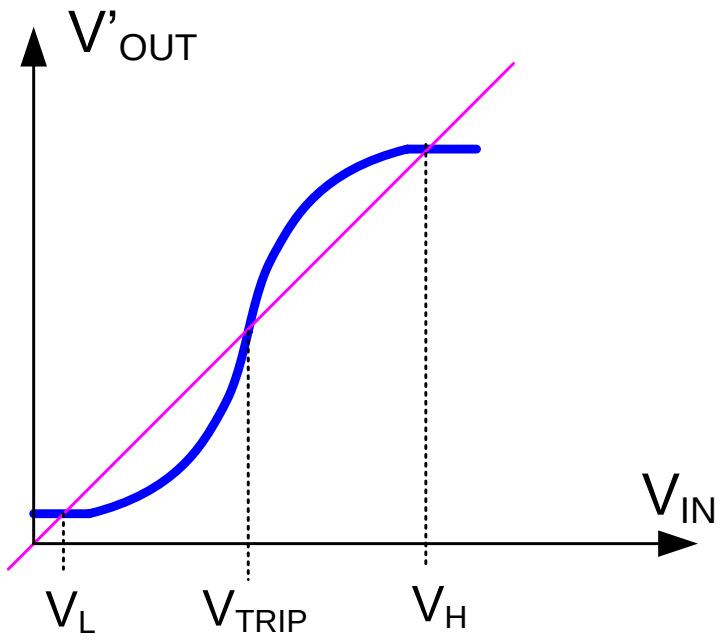


V_H and V_L often termed the "1" and "0" states

Ask the inverter how it will interpret logic levels



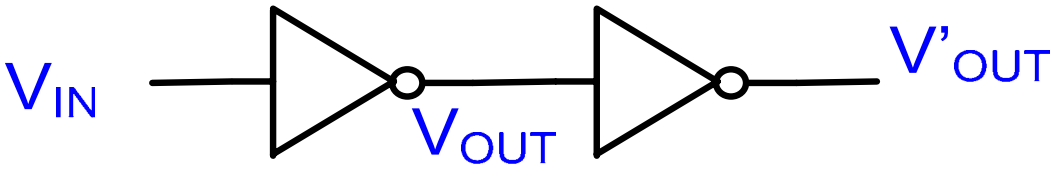
Inverter pair



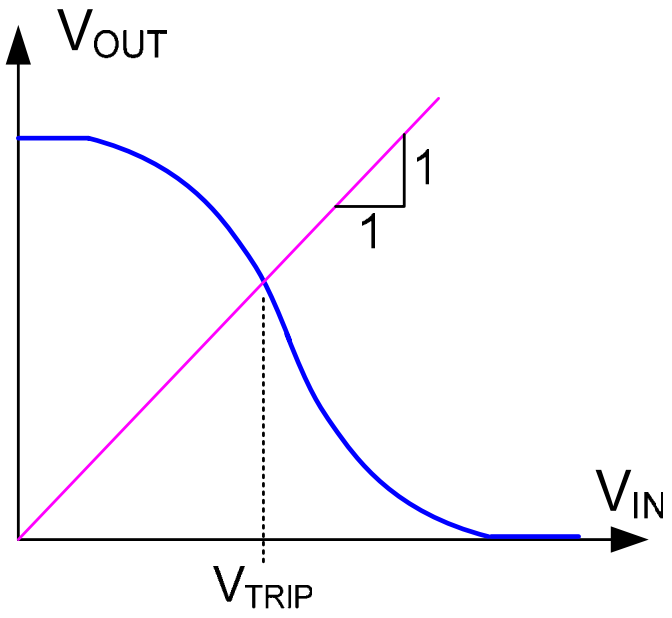
When $V'_{OUT}=V_{IN}$, V_H and V_L are stable operating points, V_{TRIP} is a quasi-stable operating point

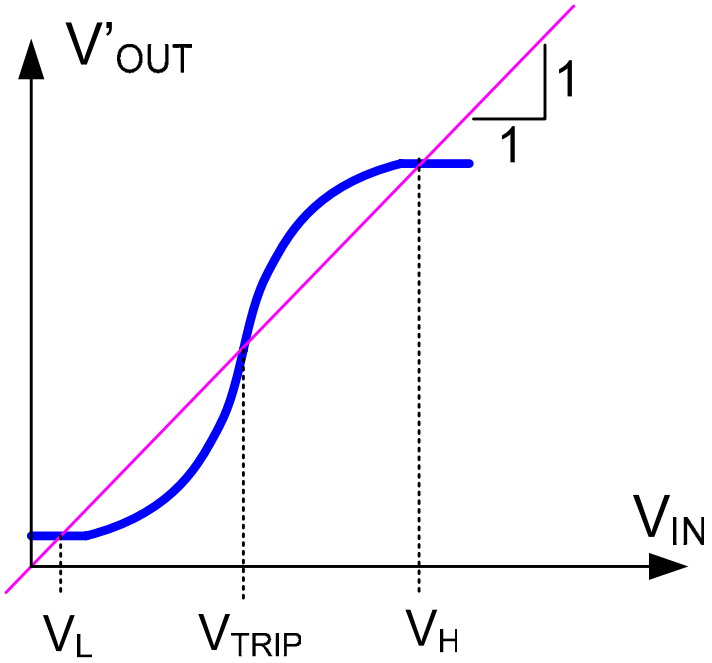
Observe: slope of IPTC is greater than 1 at V_{TRIP} and less than 1 at V_H and V_L

Observation



When $V_{OUT}=V_{IN}$ for the inverter, V'_{OUT} is also equal to V_{IN}. Thus the intersection point for $V_{OUT}=V_{IN}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{OUT}=V_{IN}$ in the inverter-pair transfer characteristics (IPTC)





Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family

What are the logic levels for a given inverter of for a given logic family?

Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line

Logic Family Characteristics

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line are V_H and V_L

Can we legislate V_H and V_L for a logic family ?

Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family

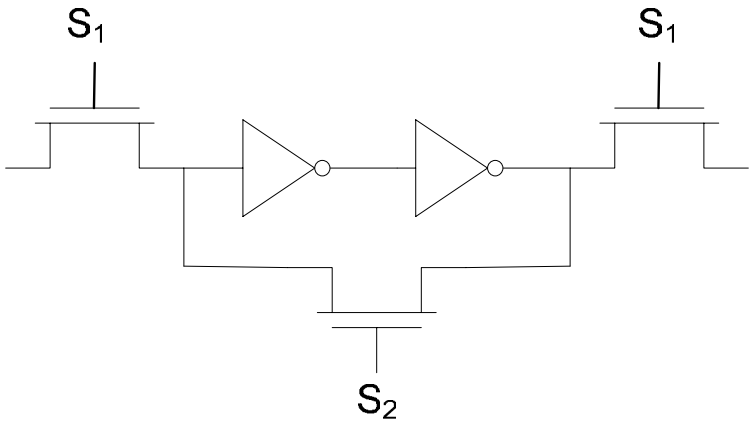
The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

What other properties of the inverter are desirable?

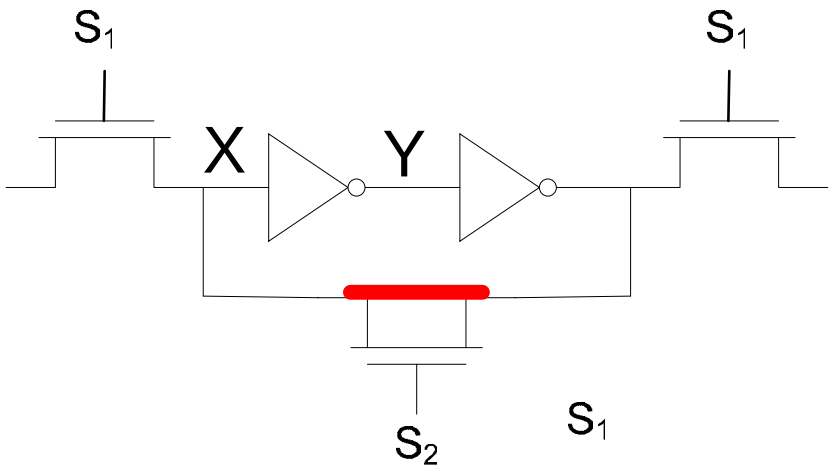
Reasonable separation between V_H and V_L (enough separation so that noise does not cause circuit to interpret level incorrectly)

$$V_{TRIP} \cong \frac{V_H + V_L}{2}$$ (to provide adequate noise immunity and process insensitivity)

What happens near the quasi-stable operating point?

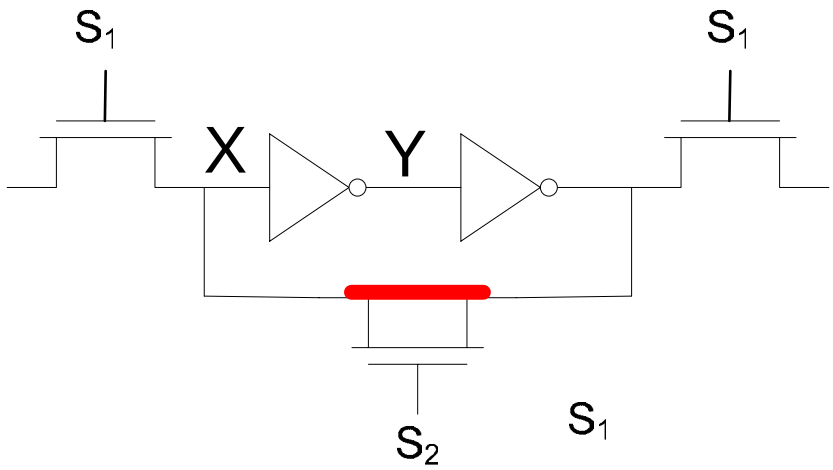


S_2 closed and $X=Y=V_{TRIP}$



What happens near the quasi-stable operating point?

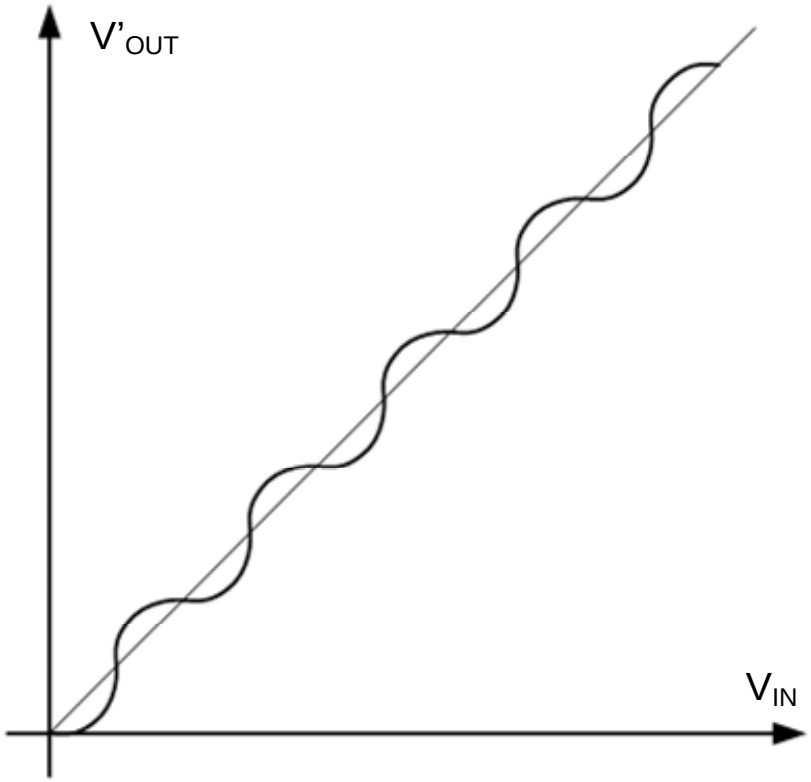
S_2 closed and $X=Y=V_{TRIP}$



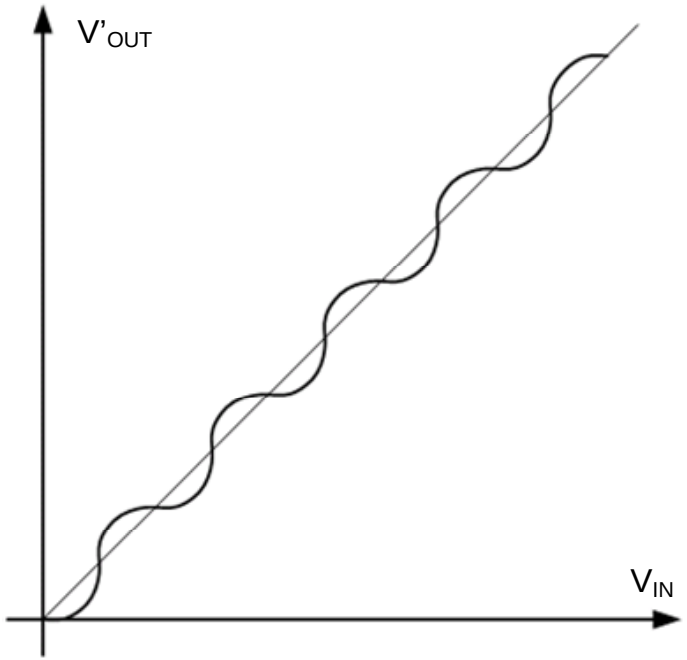
If X decreases even very slightly, will move to the X=0, Y=1 state (very fast)

If X increases even very slightly, will move to the X=1, Y=0 state (very fast)

What if the inverter pair had the following transfer characteristics?



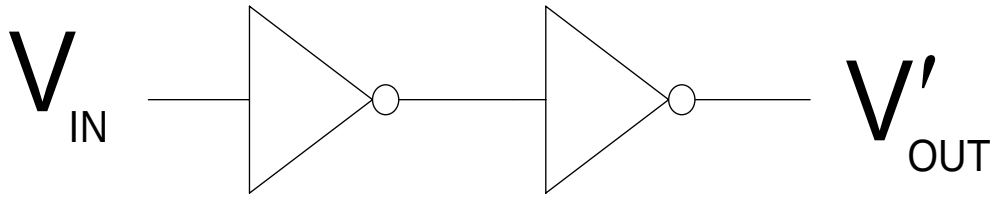
What if the inverter pair had the following transfer characteristics?



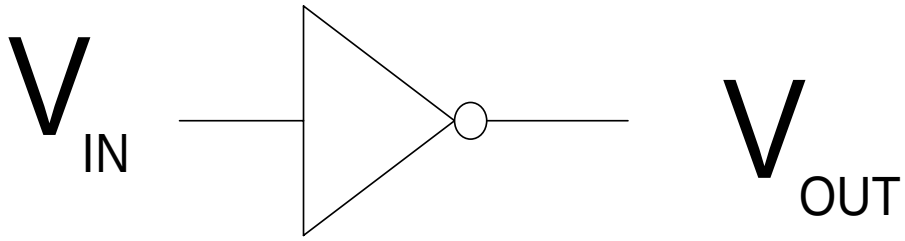
Multiple levels of logic
Every intersection point with slope <1 is a stable point
Every intersection point with slope >1 is a quasi-stable point

Del

What are the transfer characteristics of the static CMOS inverter pair?

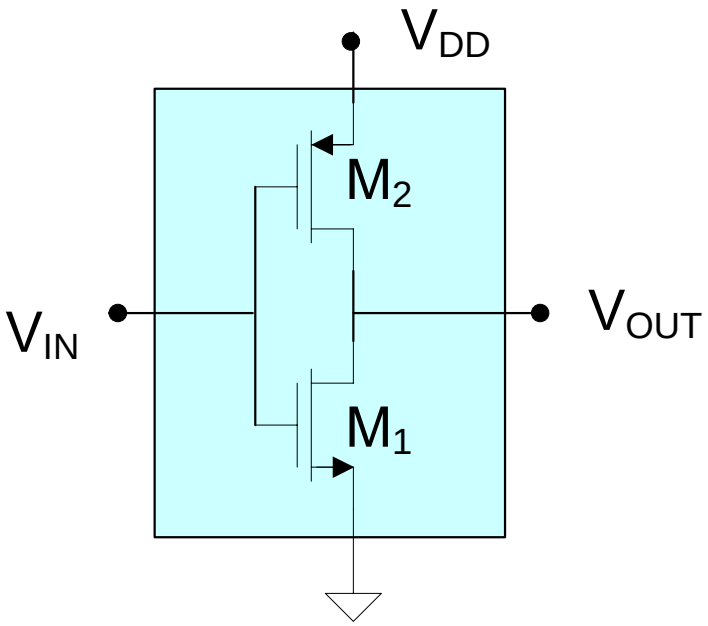


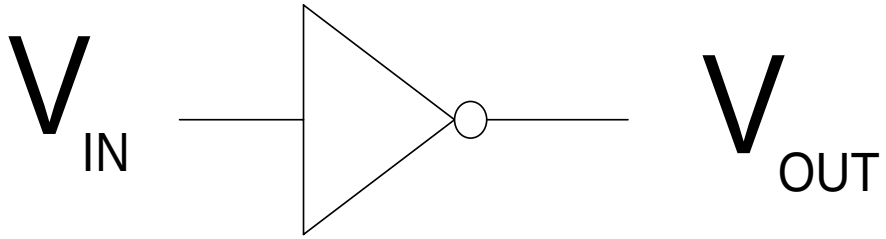
Consider first the inverter



Del

Transfer characteristics of the static CMOS inverter





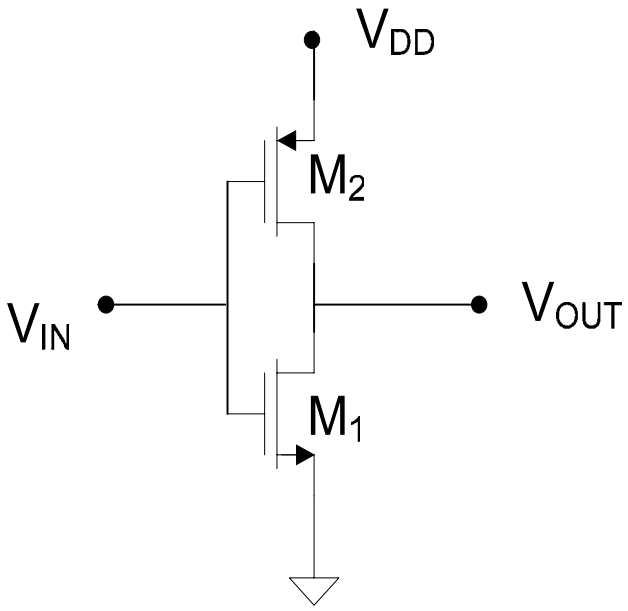
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = 0$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

It can be shown that the first solution will not verify, thus

$$V_{OUT} = 0$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

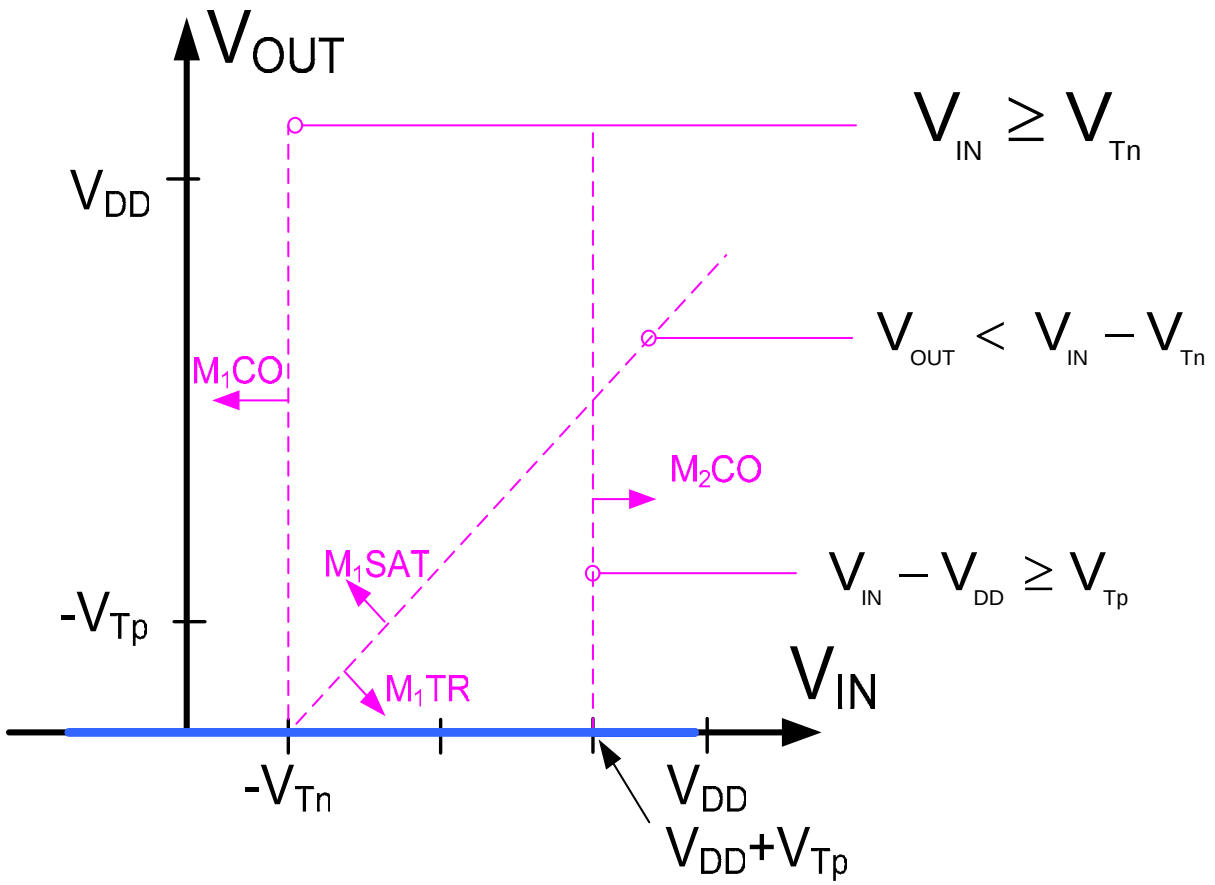
Del

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$



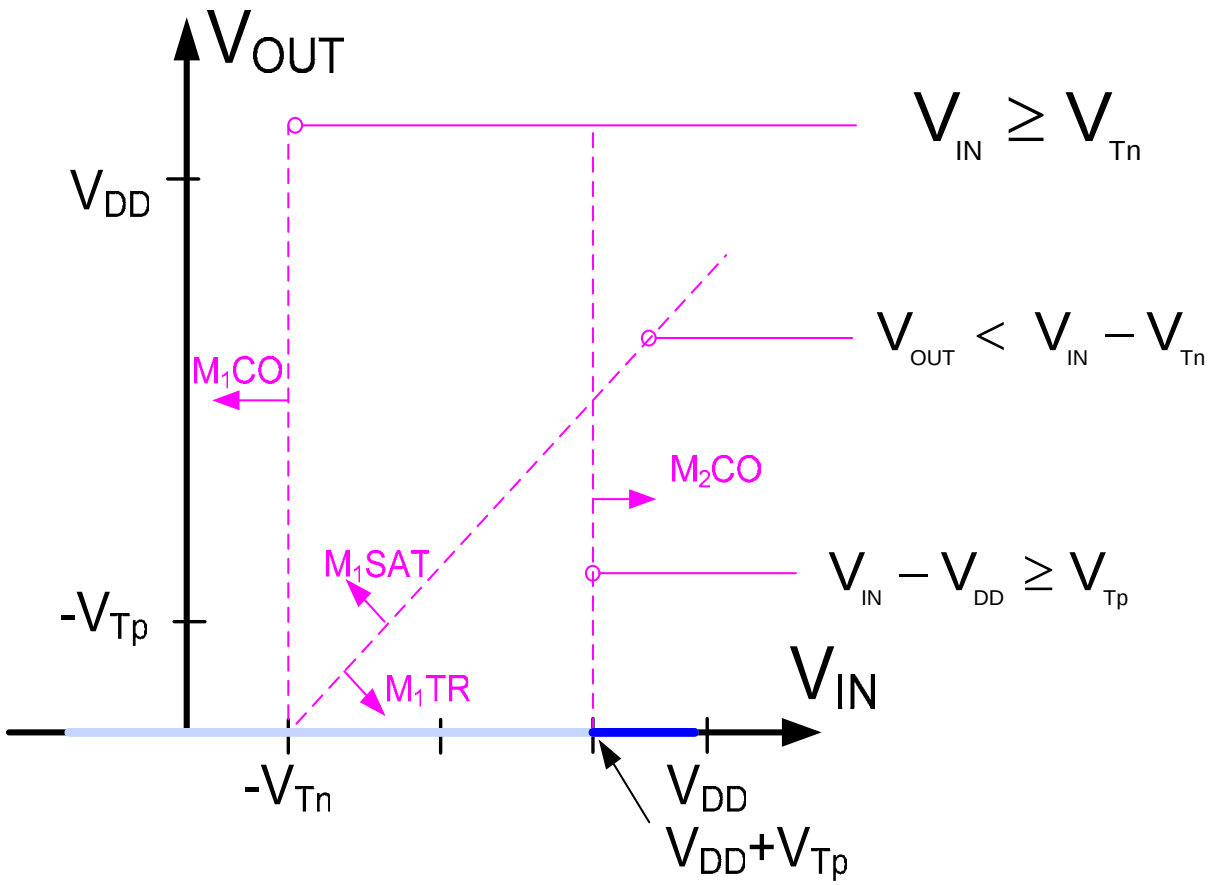
Del

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$

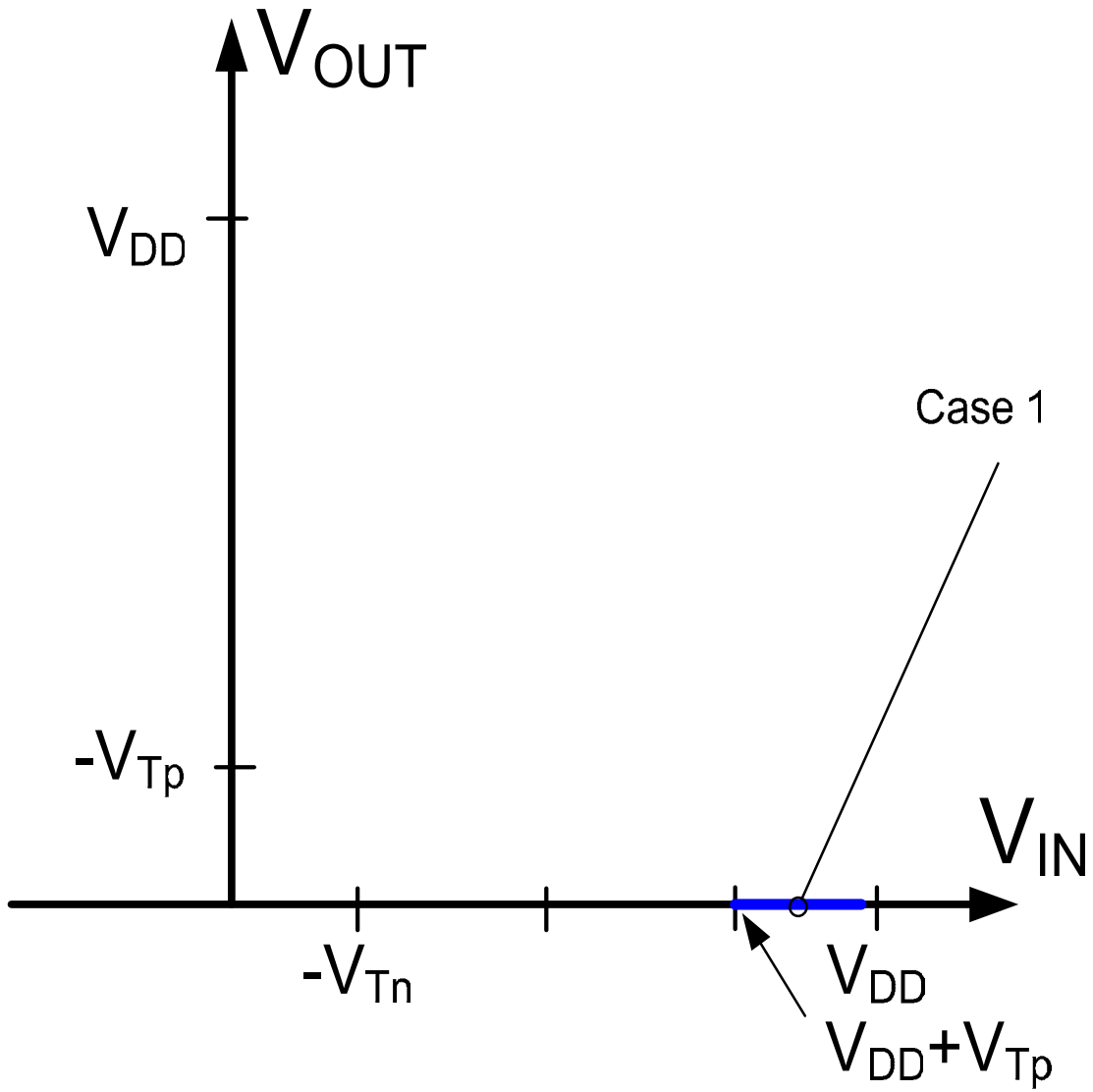


Del

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Partial solution:



Del

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 2 M_1 triode, M_2 sat